REMARKS

As a preliminary matter, a request for continued examination (RCE) is filed concurrently herewith.

I. Objections to the Drawings

According to the Office Action, the drawings are objected to under 37 C.F.R. 1.83(a) for allegedly not showing every feature of the invention specified in the claims. Specifically, it is requested that the "driver", the "driver end", the "receiver", the "receiver end", and the "signal carrying module" must be shown or the features cancelled from the claims. In response, claims 3, 4, 10, 11, 15-21, 35-36 which include these features are hereby cancelled.

II. Objections to the Claims Under 35 U.S.C. 112

According to the Office Action, claims 1-27 stand rejected under 35 U.S.C. 112, second paragraph, for allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention.

More specifically, it is alleged that claims 3, 10, and 17 are not clear regarding the first receiver and first driver being part of the first plate or if they are separate elements in the device. Claims 3, 10, and 17 are cancelled.

Also, it is alleged that claims 6, 13, and 20 are not clear regarding how can the whole first plane be a ground plane or a power plane. Claims 20 is cancelled, and claims 6 and 13 are amended to recite that the first plane is a ground plane or power plane.

Further, it is alleged that claim 8 is unclear and structurally incomplete since there needs to be a material (structural element) between the planes in order to support the via through hole. In response, claim 8 is amended to further recite "a dielectric material between the first plane and the second plane through which the plated hole extends."

In addition, claim 15 is unclear and structurally, since there needs to be a material (structural element) between the planes in order to support the via through hole. Claim 15 is cancelled.

Additionally, it is alleged that claim 34 is unclear regarding how the first layer of the printed circuit board and the second layer of the printed circuit board be adjacent layers, and still have a capacitance with plates located on these layers. In response, claim 34 is cancelled.

Finally, claims 35-36 are unclear for the reasons stated in the Office Action. These claims are cancelled.

III. Rejections of Claims Under 35 U.S.C. 102 and 103

According to the Office Action, claims 1-22, 24, 26, 28-30, and 34-40 stand rejected under 35 U.S.C. 102 for allegedly being anticipated by U.S. Patent No. 5,326,284 issued to Bohbot et al. Claims 23, 25, 27, and 31-33 stand rejected under 35 U.S.C. 103(a) as being unpatentable over the Bohbot Patent in view of U.S. Patent No. 5,475,262 issued to Wang et al. For the following reasons, these rejections are respectfully traversed insofar as they apply to the pending claims 1-2, 5-9, 12-14, 22-34, and 37-40.

As explained in the specification, it is desirable to compensate two adjacent signal paths for different odd and even mode wave velocities through a microstrip (see page 9, lines 8-9). The different velocities for the odd and even mode waves occur because the electric field associated with the odd mode wave is mostly in the air, whereas the electric field associated with the even mode wave is mostly in the dielectric (see page 6, lines 17-20). Since electric fields propagate faster through air than through a dielectric, the velocity of the odd mode is greater than the velocity of the even mode (see page 6, lines 20-21). This different in velocity between the odd mode wave and the even mode wave can lead to signal quality issues (see page 6, lines 21-25).

According to an embodiment of the invention, capacitance are placed at different locations along the signal paths (see page 9, lines 6-8). The placing of capacitance between adjacent signal paths compensates for the different odd and even mode velocities through a microstrip (see page 9, lines 8-9). Independent claims 1, 8, and 28 are amended to better define this aspect of the invention. Specifically, these claims are amended to recite "a first signal path connected to a first plane via a plurality of plated holes at different locations along said first signal path . . . a plurality of first metal floods connected to the respective plated holes to form a plurality of plates . . . a plurality of second metal floods connected to the second signal path to form a plurality of second plated above the respective first plates ..." Such newly added elements to the claims are neither described nor suggested in the cited prior art references.

The Bohbot Patent merely describes a printed circuit board having a single capacitor having a first metal flood 60 (Fig. 5a) connected to a first metal line 68 by way of metalized via R1 on plane 5b, and a second metal flood 60 (Fig. 5b) connected to a second metal line 74 on plane 5b. There is no discussion or suggestion in the Bohbot Patent of placing a plurality of such capacitors at different locations along the signal paths to reduce the difference in the velocities of the odd mode and even mode waves. Nor does the secondary reference, namely the Wang Patent, describe a plurality of such capacitors at different locations along the signal paths.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please cancel claims 3, 4, 10, 11, 15-21, 34-36 without prejudice.

Please amend claims 1, 2, 5-8, 12-14, and 28 as follows:

1. (Currently Amended) An apparatus comprising:

a first signal path connected to a first plane via a plurality of plated holes at different locations along said first signal path, the first signal path on a second plane;

a plurality of first metal floods connected to the respective plated holes to form a plurality first plates, the first metal floods on the first plane;

a second signal path on the second plane; and

a plurality second metal floods connected to the second signal path to form a plurality of second plates above the respective first plates, the second plate on the second plane.

2. (Currently Amended) The apparatus of claim 1 wherein ~~the~~ each set of first and second plates form a capacitance.

3. (Cancelled)

4. (Cancelled)

5. (Currently Amended) The apparatus of claim ~~4~~ 1 wherein the first and second signal paths are adjacent to each other.

6. (Currently Amended) The apparatus of claim 1 wherein the first plane is ~~one~~ ~~of~~ a ground plane ~~and~~ or a power plane.

7. (Currently Amended) The apparatus of claim 6 wherein each of the first metal floods is an isolated area in the first plane.

8. (Currently Amended) A method comprising:

connecting a first signal path to a first plane via a plurality of plated holes at different locations along said first signal path, the first signal path on a second plane;

forming a plurality of first plates by connecting a plurality of first metal floods to the respective plated holes, the first metal floods on the first plane; ~~and~~

connecting a plurality of second metal flood to a second signal path on the second plane to form a plurality of second plates above the respective first plates; and

a dielectric material between the first plane and the second plane through which the plated holes extend.

9. (Original) The method of claim 8 wherein the first and second plates form a capacitance.

10. (Cancelled)

11. (Cancelled)

12. (Currently Amended) The method of claim ~~11~~ 8 wherein the first and second signal paths are adjacent to each other.

13. (Currently Amended) The method of claim 8 wherein the first plane is ~~one of~~ a ground plane ~~and~~ or a power plane.

14. (Currently Amended) The method of claim 13 wherein each of the first metal floods is an isolated area in the first plane.

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Previously Added) The apparatus of claim 1 further comprising:
a dielectric layer between the first plate and the second plate.

23. (Previously Added) The apparatus of claim 2 wherein the capacitance is a buried intersignal capacitance.

24. (Previously Added) The method of claim 8 further comprising:
forming a dielectric layer between the first plate and the second plate.

25. (Previously Added) The method of cliam 9 wherein the capacitance is a buried intersignal capacitance.

26. (Previously Added) The system of claim 15 further comprising:
forming a dielectric layer between the first plate and the second plate.

27. (Previously Added) The system of claim 16 wherein the capacitance is a buried intersignal capacitance.

28. (Currently Amended) An apparatus comprising:
a printed circuit board;
a first transmission line on a first layer of the printed circuit board;
a second transmission line on the first layer of the printed circuit board; and

a plurality of capacitors connected to the first transmission line and the second transmission line at different locations, each of the capacitor comprising:

a first plate connected to the first transmission line by a plated hole, the first plate on a second layer of the printed circuit board;

a second plate connected to the second transmission line, the second plate on the first layer of the printed circuit board; and

a dielectric layer between the first plate and the second plate, the dielectric layer between the first layer of the printed circuit board and the second layer of the printed circuit board.

29. (Previously Added) The apparatus of claim 28 wherein the first plate is above the second plate.

30. (Previously Added) The apparatus of claim 28 wherein the second plate is above the first plate.

31. (Previously Added) The apparatus of claim 28 wherein the capacitor is a buried intersignal capacitor.

32. (Previously Added) The apparatus of claim 31 wherein the buried intersignal capacitor mode compensates to improve signal quality in the printed circuit board.

33. (Previously Added) The apparatus of claim 32 wherein the buried intersignal capacitor matches the propagation speed of odd-mode switch signals with the propagation speed of even-mode switch signals.

34. (Cancelled)

35. (Cancelled)

36. (Cancelled)

37. (Previously Added) The apparatus of claim 28 wherein the first transmission line is adjacent to the second transmission line.

38. (Previously Added) The apparatus of claim 28 wherein the first transmission line is inductively coupled to the second transmission line.

39. (Previously Added) The apparatus of claim 28 wherein the first transmission line and/or second transmission line are routed as microstrips.

40. (Previously Added) The apparatus of claim 28 wherein first transmission line and the second transmission line are routed on surface layers of the printed circuit board.

CONCLUSION

In view of the foregoing amendments and remarks, allowance of this patent application is respectfully requested.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box AF, Assistant Commissioner for Patents, Washington, D.C. 20231 on: April 4, 2003.

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